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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BUTLER, DENNIS	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,757	LAMBERT ET AL.	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on June 18, 2002. Claims 1-21 are pending.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title would be improved if it indicated that the memory device stores and loads the BIOS.

3. The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-12 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the phrase "said BIOS data" lacks proper antecedent basis because the previous phrase recites a BIOS program.

Claims 2-5 are rejected because they incorporate the deficiencies of claim 1.

Regarding claim 6, the phrase "said a boot operation" is unclear and lacks proper antecedent basis because no previous boot operation has been recited.

Claims 7-8 are rejected because they incorporate the deficiencies of claim 6.

Regarding claim 9, the phrase "said non-volatile memory device" is unclear and lacks proper antecedent basis because the claim recites first and second non-volatile memory devices and it is unclear which device the phrase refers to.

Regarding claim 10, the phrase "said physical data channel" lacks proper antecedent basis.

Claims 11-12 are rejected because they incorporate the deficiencies of claim 10.

Regarding claim 14, the phrases "said physical data channel" and "said physical channel" lack proper antecedent basis because the claim recites two physical data channels and it is unclear which channel the phrases refer to.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 6, 8, 15, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Stewart et al., U. S. Patent 5,815,706.

Per claims 6, 8, 15 and 17:

A) Stewart et al teach the following claimed items:

1. a microprocessor/main processor with microprocessor 300 of figures 3A and 3B;

2. a peripheral/removable storage interface with JFLK connector circuitry, with figure 2A-1, at column 10, lines 22-67 and at column 11, lines 9-20;

3. a removable storage device with the boot card and the Apollo flash shunt module at column 11, lines 1-40;

4. a controller configured to address the removable storage device to read and execute BIOS upon reset or power on of the processor/computer at column

5, lines 37-51, at column 5, line 65 – column 6, line 5, at column 10, lines 52-67, at column 11, lines 1-25 and at column 12, lines 14-27.

Per claim 18:

A) Stewart et al teach the following claimed items:

1. a host computer and a main processor with microprocessor 300 of figures 3A and 3B;

2. a removable storage interface with JFLK connector circuitry, with figure 2A-1, at column 10, lines 22-67 and at column 11, lines 9-20;

3. a removable storage device having a sectored flash memory (each set of storage locations used to store a program comprises a sector) with the boot card and the Apollo flash shunt module, at column 5, lines 37-57, at column 6, lines 6-12 and at column 11, lines 1-40;

4. reading and executing the BIOS from the removable storage device upon reset or power on of the processor/computer at column 5, lines 37-51, at column 5, line 65 – column 6, line 5, at column 10, lines 52-67, at column 11, lines 1-25 and at column 12, lines 14-27;

5. the BIOS being addressable for update through the removable storage device interface at column 5, lines 53-57, at column 6, lines 15-27 and at column 11, lines 35-40.

10. Claims 6-8, 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Bell, U. S. Patent 5,410,707.

Per claims 6, 8, 15 and 17:

A) Bell teaches the following claimed items:

1. a microprocessor/main processor with Processing Component 101 of figure 1 and at column 3, lines 55-63;

2. a peripheral/removable storage interface with memory card interface 102 of figures 1 and 2, at column 4, lines 9-43 and at column 5, lines 7-21;

3. a removable storage device with flash memory card 112 of figures 1 and 2, at column 4, lines 9-28 and at column 7, lines 1-8;

4. a controller configured to address the removable storage device to read and execute BIOS upon reset or power on of the processor/computer, at column 5, lines 22-32, at column 5, line 46 – column 6, line 2, at column 7, lines 1-8 and at column 8, lines 2-38.

Per claims 7 and 16:

Bell describes that the interface is a PC card interface at column 4, lines 34-43.

11. Claims 1, 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell, U. S. Patent 5,410,707.

Per claims 1, 4 and 14

A) Bell teaches the following claimed items:

1. a host computer/main processor with Processing Component 101 of figure 1 and at column 3, lines 55-63;

2. a removable storage interface with memory card interface 102 of figures 1 and 2, at column 4, lines 9-43 and at column 5, lines 7-21;

3. a removable storage device with flash memory card 112 of figures 1 and 2, at column 4, lines 9-28 and at column 7, lines 1-8;

4. a first memory device storing BIOS data with the portion of flash memory card storing the bootstrap code/data (the address space used in the remapped mode during initial bootstrapping) at column 5, line 53 – column 6, line 2 and at column 8, lines 6-24;

5. a second memory device storing data with the portion of flash memory card storing the data and instructions used in normal operating mode (the address space used during the normal operating mode) at column 5, lines 53-62 and at column 10, lines 32-44;

6. a physical channel (A-BUS 104) adapted to connect with a physical data channel (interface control logic 210) of the interface and shared by the first and second memory devices with figure 2 and at column 5, lines 46-65;

7. the first and second memory devices using the shared channel in the presence of signals whereby collision is avoided at column 5, lines 22-32, at column 5, line 46 – column 6, line 2, at column 8, lines 2-38 and at column 10, lines 20-54.

B) The claims seem to differ from Bell in that Bell fails to explicitly teach the second memory device storing data other than BIOS data as claimed.

C) Bell describes storing normal operating system software (BIOS) in the second memory portion (normal operation mode) at column 10, lines 47-54. However, Bell describes that flash 1 and flash 2 memories are initially erased at

column 10, lines 44-47. Therefore, Bell's normal operating system software (BIOS) in the second memory portion must include the operating system and at least one application program (data other than BIOS data) in order for the device to function properly. In addition, Bell describes locating all of the initial bootstrap data in the first memory portion and bootstrapping the host computer to an operational state with this BIOS data. The location of the additional BIOS data (data other than the initial bootstrap data) in either the first or second memory portion is a matter of design choice and it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Bell's removable storage device with all of the BIOS data in the first memory portion with the initial bootstrap data in order to separate the BIOS data from the non BIOS data and read all of the BIOS data into RAM for faster execution.

12. Claims 2-3, 5, 9-13 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell, U. S. Patent 5,410,707 in view of Robinson et al., U.S. Patent 6,279,069.

Per claims 2-3, 5, 9, 11-13 and 19-20:

A) Bell teaches the following claimed items:

1. a host computer/main processor with Processing Component 101 of figure 1 and at column 3, lines 55-63;

2. a removable storage communications interface with memory card interface 102 of figures 1 and 2, at column 4, lines 9-43 and at column 5, lines 7-21;

3. a removable storage device/memory card/PC card with flash memory card 112 of figures 1 and 2, at column 4, lines 9-28 and at column 7, lines 1-8;

4. a second/linear flash memory device storing BIOS data with the portion of flash memory card storing the bootstrap code/data (the address space used in the remapped mode during initial bootstrapping) at column 5, line 53 – column 6, line 2 and at column 8, lines 6-24;

5. a first memory device storing data with the portion of flash memory card storing the data and instructions used in normal operating mode (the address space used during the normal operating mode) at column 5, lines 53-62 and at column 10, lines 32-44;

6. a physical channel (A-BUS 104) adapted to connect with a physical data channel (interface control logic 210) of the interface and shared by the first and second memory devices with figure 2 and at column 5, lines 46-65;

7. the first and second memory devices using the shared channel in the presence of signals whereby collision is avoided at column 5, lines 22-32, at column 5, line 46 – column 6, line 2, at column 8, lines 2-38 and at column 10, lines 20-54;

8. a controller configured to address the removable storage device to read and execute BIOS upon reset or power on of the processor/computer, at column 5, lines 22-32, at column 5, line 46 – column 6, line 2, at column 7, lines 1-8 and at column 8, lines 2-38;

9. the BIOS being addressable for updating through the interface at column 3, lines 15-27.

B) The claims seem to differ from Bell in that Bell fails to explicitly teach the first memory device emulates an ATA/IDE mass storage device using sectored flash memory as claimed.

C) Bell describes storing normal operating system software (BIOS) in the first memory portion (normal operation mode) at column 10, lines 47-54. Bell does not explicitly describe that this portion emulates an ATA/IDE drive. However, Robinson teaches emulating a disk drive using a sectored flash memory with figure 2, at column 3, lines 17-35 and at column 6, line 45 – column 7, line 32. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Bell's first memory portion of the removable storage device as an ATA/IDE drive using sectored flash memory, as taught by Robinson, in order to emulate a disk drive using an array of flash memory and communicate with the host computer using the ATA/IDE protocol. One of ordinary skill in the art would have been motivated to combine Bell and Robinson because of Robinson's suggestion that flash memory arrays provide smaller and lighter functional equivalents of electro-mechanical hard disk drives at column 1, lines 36-44. It would have been obvious to one having ordinary skill in the art to combine Bell and Robinson because they are both directed to using flash memory devices as mass storage devices in computer systems.

Per claims 10 and 21:

Bell describes that the interface is a PC card interface and the card is a PC card at column 4, lines 34-43.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler
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Primary Examiner
Art Unit 2115